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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application Serial No. 10/690,029
Filing Date October 20, 2003
Inventor Garo J. Derderian
Assignee Micron Technology, Inc.
Group Art Unit 2812
Examiner Unknown
Attorney Docket No. MI22-2417
Customer No. 021567
Title: Methods of Forming Conductive Metal Silicides by Reaction of Metal with Silicon

INFORMATION DISCLOSURE STATEMENT

References -- See Attached Form PTO-1449

The attached form PTO-1449 is submitted in compliance with 37 CFR §1.56. Pursuant to 1276 OG 55, August 5, 2003, no copies of cited U.S. patents or U.S. patent application publications are included, as the date of filing of this patent application occurs after June 30, 2003. Copies of all other references are attached. No admission is made regarding whether all the listed references are prior art.

Citation of the referenced art is respectfully requested.

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Respectfully submitted,

Dated: 9/2/04

By: [Signature]
Mark S. Matkin
Reg. No. 32,268



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PTO/SB/21 (6-98)
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	Filing Date	October 20, 2003
	First Named Inventor	Garo J. Derderian
	Group Art Unit	2812
	Examiner Name	Unknown
Total Number of Pages in This Submission	Attorney Docket Number MI22-2426	

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MI22-2426SERIAL NO.
10/690,029LIST OF ART CITED BY APPLICANT
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APPLICANT: Garo J. Derderian

FILING DATE
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2812

U.S. PATENT DOCUMENTS

*Examiner's Initials		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	4,086,074	04/78	Minot et al.			
	AB	4,622,735	11/86	Shibata			
	AC	4,683,645	08/87	Naguib et al.			
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							Yes	No
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	AK							
	AL							

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	AM		ABSTRACT: Basceri et al., Atomic Layer Deposition for Nanoscale CU Metalization, 10 pages (pre-April 2004).
	AN		En et al., Plasma immersion ion implantation reactor design considerations for oxide charging, 85 SURFACE AND COATINGS TECHNOLOGY 64-69 (1966).
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EXAMINER		DATE CONSIDERED	

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*Examiner's Initials		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,670,298	09/97	Hur			
	AB	6,037,239	03/00	Jennings			
	AC	6,096,621	08/00	Jennings			
	AD	6,130,140	10/00	Gonzalez			
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	AI	6,277,728 B1	08/01	Ahn et al.			

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	AK							
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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

	AM		ABSTRACT: How to Eliminate Voiding in Porous-Low-k Dielectrics and The Mechanism of Void Formation; Lin et al.; 4 pages
	AN		COB Stack DRAM Cell Technology beyond 100 nm Technology Node; Yongjik Park & Kinam Kim; pp. 349.1 - 349.3;
	AO		Rubin et al., Shallow-Junction Diode Formation by implantation of Arsenic and Boron Through Titanium-Silicide Films and ..., 17 IEEE Transactions on Electron Devices, No. 1, pp. 183-190 (January 1990).
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	AA	6,440,793 B1	08/02	Divakaruni et al.			
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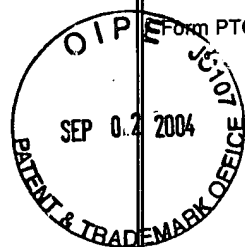
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

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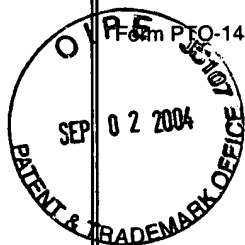
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